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Mark A. Litman & Associates, P.A.
3209 West 76th St.
Suite 205
York Business Center
Edina, MN 55435

EXAMINER	
HSU, RYAN	

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BEFORE THE BOARD OF PATENT APPEALS AND INTERFERENCES

Application Number: 10/764,827
Filing Date: January 26, 2004
Appellant(s): SMITH ET AL.

Mark A. Litman
For Appellant

EXAMINER'S ANSWER

This is in response to the appeal brief filed July 7th, 2007 appealing from the Office action mailed December 13th, 2006.

(1) Real Party in Interest

The real part in interest is identified by the appellant's Appeal Brief as Shuffle Master, Inc., the assignee of the full right, title and interest in this application and has a place of business at 1106 Palms Airport Drive, Las Vegas, Nevada 89119-3730.

(2) Related Appeals and Interferences

The examiner is not aware of any related appeals, interferences, or judicial proceedings which will directly affect or be directly affected by or have a bearing on the Board's decision in the pending appeal.

(3) Status of Claims

The statement of the status of claims contained in the brief is correct.

(4) Status of Amendments After Final

The appellant's statement of the status of amendments after final rejection contained in the brief is correct.

(5) Summary of Claimed Subject Matter

The summary of claimed subject matter contained in the brief is correct.

(6) Grounds of Rejection to be Reviewed on Appeal

The appellant's statement of the grounds of rejection to be reviewed on appeal is correct.

(7) Claims Appendix

The copy of the appealed claims contained in the Appendix to the brief is correct.

(8) Evidence Relied Upon

6,607,443	Miyamoto et al.	8-2003
5,497,461	Matsumoto et al.	3-1996

(9) Grounds of Rejection

The following ground(s) of rejection are applicable to the appealed claims:

Claim Rejections - 35 USC § 102

Claims 1-5, 7-24, and 41 are rejected under 35 U.S.C. 102(e) as being anticipated by Miyamoto et al. (US 6,607,443 B1).

Regarding claims 1, 22, and 41, Miyamoto discloses an automated gaming system comprising a gaming table and an upright video display panel comprising: (a) an upright video display panel, the panel displaying a virtual image of a dealer (*see Fig. 7 and the related description thereof*); (b) a table having an upper surface, the upper surface having a substantially horizontal video display surface that provides a continuous field of video display and at least two different player positions (*see elements [10-12] of Fig. 1 and the related description thereof*); (c) at least one player position having at least one local processor dedicated to the at least one player position that is capable of executing code (*see sub-cpu [204] and main cpu [201] of Fig. 15 and the related description thereof*) and (d) at least one main game processor and optionally at least one additional game display processor in information communication with the upright video display panel and the video display surface, the main processor or at least one display processor directing video display on both the upright video display panel and the video display surface, and the main game processor providing game rules for the play of at least one casino table card game without the use of physical cards on the table (*see Fig. 3-4 and the related description thereof*).

Additionally, Miyamoto discloses a gaming system that comprises a plurality of player stations, each player station having its own manufactured intelligence, which is a processor that executes code (*see col. 14: ln 4-49*). If manufactured intelligence is defined as the ability to execute code than it is inherent in the invention of Miyamoto. As each player station contains several sensing devices for each player station to place inputs to interact with the game. However, although not explicitly stated by the Miyamoto reference for this ability every electronic sensor component must be attached to some sort of interface processing board. Furthermore, even the most simple signal interface boards contain the ability to execute code. As signals are basically encoded from one language (*ie: the physical input*) into the electronic symbol (*ie:* .the analog or digital signal) these basic types of translations incorporate a basic instruction set and would in the broadest reasonable interpretation constitute the ability to execute code.

Regarding claim 2, Miyamoto discloses a gaming system wherein each player position has an individual player processing board that is capable of executing code and is dedicated to that position (*see Figs. 9, 13 and the related description thereof, col. 2: ln 41-64*).

Regarding claim 3, Miyamoto discloses a gaming system wherein each individual player processing board that executes code will also communicate directly with the main game processor (*see col. 2: ln 41-64, sub-cpu and main cpu interaction of Fig. 15 and the related description thereof*).

Regarding claims 4-5, Miyamoto discloses a gaming system wherein each individual player processing board communicates directly with a single Dealer game engine processor or communicates directly with the display processor (*see col. 4: ln 17-35*).

Regarding claims 7-10, Miyamoto discloses a gaming system wherein the video display surface has changeable light filtering that can screen displayed images from various angles (*ie: video display is capable of being controlled to change alter the pixels and may be viewed from various angles*) (*see display [7] of Fig. 1 and the related description thereof, col. 5: ln 1-54*). Additionally, Miyamoto discloses a system wherein the light filtering can be changed upon command by a processor or by an external command. Furthermore, Miyamoto discloses a gaming system wherein player input is provided at least in part by controls in the video display surface (*see Fig. 13 and the related description thereof*).

Regarding claim 11, Miyamoto discloses a gaming system wherein the controls comprise touch screen controls (*see Fig. 13 and the related description thereof, col. 14: ln 16-49*).

Regarding claim 12, Miyamoto discloses a gaming system wherein the controls comprise a panel embedded into the video display surface (*see Fig. 19(a-b) and the related description thereof*).

Regarding claims 13-15, Miyamoto discloses a gaming system wherein additional player input can be provided from player input or player controls provided on a surface below the video display surface and facing a position where players are to be seated (*see Fig. 20 and 23 and the respective related description thereof, element [401(a-c)] of Fig. 24 and the related description thereof*).

Regarding claims 16-19 and 21, Miyamoto discloses a gaming system wherein communication between the main game processor and each local processor is performed through a transaction-based protocol (*see col. 15: ln 25-50*). Additionally, Miyamoto discloses a system

wherein either the main game processor or local processing board can start a transaction (*see CPU block [20] and player terminal [10] of Fig. 4 and the related description thereof*).

Regarding claim 20, Miyamoto discloses a gaming system wherein each player position has a local processor comprising an individual player processing board dedicated to that position and communication between the main game processor and the individual player processor is performed through a transaction-based protocol (*ie: the play of the game is based upon certain conditions and input/output responses made by the player or game program*)(*see col. 15: ln 25-50*).

Regarding claim 23, Miyamoto discloses a device wherein each player station and the main game processor are in communication (*see CPU.[20] and player terminal [10] of Fig. 4 and the related description thereof*).

Regarding claim 24, Miyamoto discloses a device wherein the communication is event driven (*ie: a processor controls the actions of the game when different inputs are received to advance a game*) (*see col. 15: ln 25-50*).

Claim Rejections - 35 USC § 103

Claims 25-40 are rejected under 35 U.S.C. 103(a) as being unpatentable over Miyamoto et al. (US 6,607,443 B1) in further view of Matsumoto et al. (US 5,497,461 A).

Regarding claim 26, Miyamoto discloses a gaming system comprising a gaming table and an upright video display panel comprising: (a) an upright video display panel, the panel displaying a virtual image of a dealer (*see Fig. 7 and the related description thereof*); (b) a table having an upper surface, the upper surface having a substantially horizontal video display surface that provides a continuous field of video display and at least two different player positions (*see*

elements [10-12] of Fig. 1 and the related description thereof), each player position having an intelligent board that executes code; and (c) at least one main game processor and optionally at least one additional game display processor in information communication with the upright video display panel and the video display surface, the main processor or at least one display processor directing video display on both the upright video display panel and the video display surface, and the main game processor providing game rules for the play of at least one casino table card game without the use of physical cards on the table (*see Fig. 3-4 and the related description thereof*); (d) wherein the intelligent boards are in communication with the main game processor, sending packets of information from player positions as events occur (*see col. 14: ln 4-49*). However, Miyamoto is silent with regard to incorporating sending the information in the form of packets. However, in the network arts it is inherent to establish a protocol in which communication between two processors or devices may occur in a system. One of the most common ways is using network packet that encapsulates information in a way that is consistent and accurate and therefore the data will properly reach its destination. In a related gaming patent, Matsumoto et al. teaches the implementation of monitoring packet information while transmitting data from one processor to another (*see Fig. 11 and the related description thereof*). Matsumoto teaches the implementation of packets to allow several different processors to know when the information received is for them to act upon (*see Fig. 12 and the related description thereof*). One would be motivated to incorporate such a feature in order to allow for distributed computing to occur which would allow for several processors to communicate with one another. Therefore it would have been obvious to one of ordinary skill in the time the invention was made to

incorporate a packet system to send information from the main processor to the player station at the time the invention was made.

Regarding claim 27, Miyamoto discloses a gaming system wherein the communication between the intelligent boards and the main game processor comprises communication of player input (*see CPU [20] and player terminal [10] of Fig. 4 and the related description thereof*).

Regarding claim 28, Miyamoto discloses a gaming system wherein there is a dealer game engine intermediate the intelligent boards and the main game processor (*see CPU [20] and player terminal [10] of Fig. 4 and the related description thereof*).

Regarding claim 29, Miyamoto discloses a gaming system wherein there is a direct line of communication between the intelligent boards and the main game processor for communication of player input (*see CPU [20] and player terminal [10] of Fig. 4 and the related description thereof*).

Regarding claim 31, Miyamoto teaches a method of playing an automated game having an upright video display panel, the panel displaying a virtual image of a dealer (*see Fig. 7 and the related description thereof*), a table having an upper surface, the upper surface having a substantially horizontal video display surface that provides a common video display viewable from all player positions and at least two different player positions, each of the at least two player positions having an intelligent board (*see elements [10-12] of Fig. 1 and the related description thereof*), and a main game processor, the method comprising sending information from intelligent boards that executes code at player positions to the main game processor as events occurs at player positions (*see Fig. 3-4 and the related description thereof*). However, Miyamoto is silent with regard to incorporating sending the information in the form of packets.

However, in the network arts it is inherent to the art to establish a protocol in which communication between two processors or devices may occur in a system. One of the most common ways is using a network packet that encapsulates the information in a way that is consistent and accurate and therefore the data will properly reach its destination. In a related gaming patent, Matsumoto et al. teaches the implementation of monitoring packet information while transmitting data from one processor to another (*see Fig. 11 and the related description thereof*). Matsumoto teaches the implementation of packets to allow several different processors to know when the information received is for them to act upon (*see Fig. 12 and the related description thereof*). One would be motivated to incorporate such a feature in order to allow for distributed computing to occur which would allow for several processors to communicate with one another. Therefore it would have been obvious to one of ordinary skill in the time the invention was made to incorporate a packet system to send information from the main processor to the player station at the time the invention was made.

Regarding claim 32, Miyamoto teaches a method wherein player input initiates the communication between the intelligent boards and main game processor (*ie: the player input initiates play of the game through a wager; see CPU [20] and player terminal [10] of Fig. 4 and the related description thereof*).

Regarding claim 33, Miyamoto teaches a method wherein there is a dealer game engine intermediate the communication path between the intelligent boards and the main game processor (*see CPU [20] and player terminal [10] of Fig. 4 and the related description thereof*).

Regarding claim 34, Miyamoto teaches a method wherein the packets of information are sent directly from the intelligence boards from the intelligence boards to the main game

processor for communication of player input (*see CPU [20] and player terminal [10] of Fig. 4 and the related description thereof*).

Regarding claims 35 and 38, Miyamoto teaches a method wherein the communication is event driven (*ie: a processor controls the actions of the game when different inputs are received to advance a game*) (*see col. 15: ln 25-50*).

Regarding claim 36 and 39, Miyamoto teaches a method wherein the communication comprises a cyclic redundancy check (*see CPU [20] and player terminal [10] of Fig. 4 and the related description thereof*). Miyamoto is silent with regard to the communication comprising a cyclic redundancy check. However Miyamoto teaches a system that incorporates communication between a CPU and a player station. It is an inherent problem in the networking field that information can be lost transferring from one point to another. One of the solutions is a cyclic redundancy check that allows the data integrity to be checked and validated. The incorporation of a cyclic redundancy check into a communication is old and well known in the art of communication systems and would therefore be obvious to one of ordinary skill in the art at the time the invention was made to incorporate in order to protect and check the data being transferred within the system.

Regarding claim 37 and 40, Miyamoto teaches a method wherein the communication is transaction based (*ie: the play of the game is based upon certain conditions and input/output responses made by the player or game program*)(*see col. 15: ln 25-50*).

Regarding claims 25 and 30, Miyamoto teaches a device wherein information communicated is included in an information packet (*see Fig. 4 and the related description thereof*). However, at the time the invention was made it is old and well known in the

communication arts to formulate information packets in order to transfer information. It would not be possible to transfer data from one device to another without a protocol such as a packet to transport the data. Therefore as taught by Matsumoto above, it would have been obvious to one of ordinary skill in the art at the time the invention was made to incorporate the use of packets while transferring data from one processor with the system of Miyamoto in order to communicate with the intelligent boards.

(10) Response to Argument

Technical Background

Definitions:

Code (taken from www.wikipedia.org)**:** In communications, a **code** is a rule for converting a piece of information (for example, a letter, word, or phrase) into another form or representation, not necessarily of the same type. In communications and information processing, **encoding** is the process by which information from a source is converted into symbols to be communicated.

Signal Processing (taken from www.wikipedia.org)**:** is the analysis, interpretation and manipulation of signals. Signals of interest include sound, images, biological signals such as ECG, radar signals, and many others. Processing of such signals includes storage and reconstruction, separation of information from noise (e.g., aircraft identification by radar), compression (e.g., image compression), and feature extraction (e.g., speech-to-text conversion).

-Applicant argues that Miyamoto does not disclose/anticipate the limitation of a gaming device wherein "at least one player position having at least one local processor dedicated to the at least one player position that is capable of executing code".

Regarding arguments with respect to claims 1, 22, and 41, on page 12 of the Appeal Brief filed by the appellant's challenges that Miyamoto et al. fails to meet the limitation of "at least one player position having at least one local processor dedicated to the at least one player position having at least one local processor dedicated to the at least one player position that is capable of executing code". Examiner respectfully disagrees.

The reference of Miyamoto encompasses these claims in two different interpretations as the language construed by the instant claims allows for multiple interpretations. In the first interpretation Miyamoto's that meets the criteria set forth by the instant limitation as seen in the distinction Miyamoto makes between the game program being processed by the main-CPU [201] (*see Fig. 4 and the related description thereof*) and a separate sub-CPU which has been termed as the SMPC (System Manager & Peripheral Control) (*see col. 5: ln 20-26*). As defined, its functions include collecting sound recognition signals from the sound recognition circuit [15] or image recognition signals from the image recognition circuit [16] in response to requests from the main CPU (*see col. 5: ln 20-25*). With this relationship it is clear that two processors exists one that is the main game processor with the option to incorporate a game display processor (*see video block [21] of Fig. 4 and the related description thereof*) and the other a sub-CPU that is dedicated to servicing the operations requested by the individual player terminals. Additionally,

it is noted that each player station comprises its own individual image and sound recognition circuits that are specifically dedicated to each player position and in communication with the sub-CPU (*see element [13-16] of Fig. 4*). Therefore the limitation of "at least one player position having at least one local processor dedicated to the at least one player position (*ie: the sub-CPU is dedicated to the processing of information from each of the different player positions*) and is capable of executing code" (*ie: inherent attribute of processors. Additionally, processing of signals and interaction between the sub-CPU and main-CPU would meet this limitation*) is anticipated by the prior art reference of Miyamoto.

In the alternative interpretation, which has been contested by the appellant is to viewed the "image and sound recognition circuits" (*see element [13-16]*) themselves as capable of meeting the limitation of "at least one player position having at least one local processor dedicated to the at least one player position that is capable of executing code". The reasoning behind this interpretation is based on the definitions provided by the appellant's own specification and basic definitions of electrical systems. At the root, the definition of code is simply as defined in wikipedia: "a rule for converting a piece of information into another form or representation". Therefore the limitation "capable of executing code" would be interpreted as would be anticipated by the Miyamoto reference with the incorporation of the image and sound recognition circuit, since it is capable of executing rules in translating physical inputs from each player position into electrical signals that are then forwarded to the sub-CPU and main-CPU to be used in the main game. Additionally, the reasoning given above, still meets the interpretation proposed by the appellants brief which states that the "execution of code" requires the ability "to

receive data, perform an intelligent operation on that data through data processing techniques and to forward or store the processed data". As the conversion of the inputs received from physical inputs into an electronic signal would be considered an intelligent operation the image and sound recognition circuits, contrary to the appellant's arguments would meet this limitation. With respect to Miyamoto the image and sound recognition circuits perform the translation of the different inputs that would need to be **encoded** in a manner as to fairly represent what command the player has made. For example, if a player makes a "STAND" command by moving his/her hand across the sensor, the circuitry would translate the information into the "code" as an 'electrical signal' so that the electric gaming device would be able to understand the operate on the command (*see col. 14: ln 4-49*) or at the very least make it useable for the information to be read by the main-CPU. As additional support that the circuitry can be interpreted as a processor that is capable of executing "code" is that the sound recognition circuit [15] as disclosed in Miyamoto is able to process and "recognizes which of [the] prescribed reference level bands the level of an input sound signal corresponds to, and outputs the sound recognition outcome as sound recognition signals". As such, it can be interpreted that Miyamoto does in fact, via the image and sound recognition circuits meet the claim limitation of "at least player position having at least one local processor dedicated to the at least one player position that is capable of executing code.

-Appellant argues that the system of Miyamoto has multiple player positions that have a communal processor (the motherboard [6]) is not dedicated to the at least one player position.

On page 12 of the Appellant's Brief, the Appellant asserts that the construction offerred by Miyamoto of a communal processor (the motherboard 6) is not dedicated to the at least one player position. Examiner respectfully disagrees. The limitation that a processor is dedicated to at least one player position is still encompassed by being shared by multiple positions. As if a processor (*ie: the sub-CPU*) is dedicated to each player position that contains the signaling circuitry then it meets the condition of having at least one processor that is dedicated to the at least one player position. The limitation as exists, does not require a one to one ratio of player position but is also subject to the interpreation of one processor to many player positions due to the applicant's use of "**at least one processor....that is dedicated to the at least one player position**".

-Appellent argues that Miyamoto to which the Office Action have referred of an intelligent device is not dedicated to a player position and not provided in the prior art's disclosure. Furthermore, it is noted that each of the elements cited is a 'dumb' element and does not execute code.

On page 14 of the Appellant's Brief, the Appellant asserts that Miyamoto only contains "dumb" elements at each of the player positions and the signaling circuits are only switches or buttons and therefore do not constitute an "intelligent" device. Examiner respectfully disagrees. As defined by the applicant's specification "the individual player positions have a separate intelligence at each player position that accepts player input and communicates directly with a

game engine (main game computer or processor). The intelligence is preferably an intelligent board that **can process information**. For purposes of this disclosure the term "intelligent" refers to the ability to **execute code, either provided in the form of software or hardware circuits**" (*see paragraph [0052] of US Publication (2005/0164759 A1)*. As pointed above, the image and sound recognition circuits are hardware circuits that can process information. They are able to translate and execute code as to translate the signals into a binary code (basic communication of computer language that informs the computer of instructions through strings of 1's and 0's) that is useable in the electronic gaming device. It is further noted that in direct contradiction to the appellant's arguments concerning "intelligent" devices, it is stated in the applicant's specification that such processing may at least comprise "some of signal converting (e.g., signals from player card readers, credit deposit, currency readers, coin readers, touch screen signals, control panel signals) into a signal that can be included in an information packet" (*see paragraph [0052]*).

-Appellant argues with respect to claims 25 and 30-40 as being a failed rejection to provide references that specifically identify local processing boards dedicated to individual player positions.

On page 16, the Appellant's Brief reiterates the arguments the appellants representative has made with respect to Miyamoto and have already been addressed above.

-Appellant has incorporated a restatement of arguemnts made in the last response.

On page 17-19 of the Appellant's Brief, the Appellant restates the arguments presented as a response to the last rejection. The Examiner has incorporated the same arguments that were previously presented to the Appellant.

"Applicant's arguments have been fully considered but they are not persuasive. The applicant's representative contends that the prior art of Miyamoto lacks in disclosing any type disclosure or teaching of the applicant's "manufactured intelligence". Although the applicant's opinions have been noted and fully considered, the Examiner respectfully disagrees. The term of contention the applicant's representative has stated in the remarks is that intelligence is defined as "**the ability to execute code**". If this is the definition of the applicant's intelligence in their invention then it can be defined as any processor or any processing component in modern computing systems. It is an inherent property in modern processors to accept signals or execute code in the form of software or hardware circuits. If a processor did not have the ability to execute code or software or information from hardware circuits, then it would not be able to perform any operations. Therefore Miyamoto's system meets the criteria set form by the applicant's claims, since it provides a plurality of individual terminals, which are in communication with a main CPU that processes the operations of the game and is in communication with the individual local processors (*ie: sub-CPU*) which handle the player input responses to allow the operation of the game to occur. By the definition of intelligence set forth above, all processors disclosed and taught in Miyamoto inherently have the ability to execute code, since they are responsible for the processing of a game program in order to

operate a game. Additionally, Examiner also directs the applicant's representative to independent claims 1, 22, 26, and 41, which have been examined as apparatus claims. The prior art of record, Miyamoto operates and performs a game with a video display and a plurality of player terminals. The contention that the processors do not have manufactured intelligence (*ie: ability to execute code*) is a moot point since the processors of Miyamoto are still capable of having manufactured intelligence and therefore anticipate the instant invention (*see MPEP 2112, In re Schreiber, 128 F.3d at 1478, 44 USPQ2d at 1432*). Finally, the applicant's representive attacks that Miyamoto's player terminal processor little more than 'button' functions, such that when stimulated an electrical signal is sent. However, the invention of Miyamoto is able to sense the movements and desired operations of a player. The applicant's representative is correct in the fact that signals are sent from the input/output devices, however, they are then collected and processed in order to cause an effect in the game program. By the definition set forth by the applicant's representative "the ability to execute code" these processors translate the signals and then translate the information into the game which would require using code to communicate between the hardware signals and the game program. However, the Examiner directs the applicant to its own contradiction that Miyamoto fails to meet the criteria set forth by the claim limitations. In applicant's own specification intelligence is described as "the ability to execute code, either provided in the form of software or hardware circuits. Such processing may at least comprise some of **signal converting** (e.g., signals from player card readers, credit deposit, currency readers, coin readers, touch screen signals, control panel signals) into a signal that can be included in an information packet and interpreted by the main game computer when the signal is sent". Miyamoto meets this criteria by using

"recognition circuits" to translate the information into command or response that is useable in the game program".

(11) Related Proceeding(s) Appendix

No decision rendered by a court or the Board is identified by the examiner in the Related Appeals and Interferences section of this examiner's answer.

For the above reasons, it is believed that the rejections should be sustained.

Respectfully submitted,

Ryan Hsu

Assistant Examiner

Conferees:

Robert E. Pezzuto

Supervisory Primary Examiner, AU 3714

Xuan M. Thai

Supervisory Primary Examiner, AU 3714